Digital Logic
EE 354

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Office Hours: 1:00 PM-1:30 PM, MTWR


OUTLINE
1. Number Systems
2. Boolean Algebra
3. Simplification of Boolean Function by Karnaugh Map
4. Combinational Logic Circuits Design and Analysis
5. Sequential Circuits Design and Analysis
6. Registers and Counters
7. Programmable Logic Circuits
8. Verilog VHDL

Grading Policy
- Quizzes: 80%
- Final Exam: 20%