Syllabus
Computer Architecture EE/CS 458

Instructor: Dr. Hosseini
Office: EMS 1091
Phone: (414)-229-5184
E-Mail: hosseini@uwm.edu

Office Hours: 11:00 AM-12:00 PM, TR

Prerequisite: Jr. St; Digital Logic EE 354 and either Computer Organization and Assembly Language Prog. CS 315 or Microprocessors EE 367.


OUTLINE
1. Introduction
2. Register Transfer Language
3. Basic Computer Organization and Design
4. Instruction Set Architecture
5. Control Unit Design
6. Pipelining
7. Computer Arithmetic and ALU Design
8. Input and Out Organization
9. Memory Organization
10. Introduction to Parallel Computer Architecture

Grading Policy for Undergraduate Students
- Homework: 10%
- Exam I: 25%
  Exam II: 25%
- Final Exam: 40%

Grading Policy for Graduate Students
- Homework: 10%
- Exam I: 20%
- Exam II: 20%
- Project: 20%
- Final Exam: 30%